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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,528	11/20/2001	Tomokazu Kakumoto	018656-248	8861

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EXAMINER	
LAM, HUNG H	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,528	KAKUMOTO ET AL.	
	Examiner	Art Unit	
	Hung H. Lam	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *6-9,11-17,20-26,28-30 and 32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10,18,19,27 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/20/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

2. Claims 6-9,11-17,20-26,28-30 and 32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 12/09/04.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1,2,4,5, and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsushima et al. (US6,396,468).

With regarding to **claim 1**, Matsushima discloses a scanning circuit, comprising:

a plurality of transfer stages connected in series, each of which receives an input signal (Fig. 6; Input signal SPG; GS-P to GS-257 are interpreted as transfer stages) and produces a corresponding output signal in response to a clock signal (Figs. 6 and 7; Col. 12, Ln. 23-27).

an output circuit which logically combines the output signals of said transfer stages with another signal to generate scanning pulses (Fig. 6; AND1-256 circuits; e.g. Q1 is combined with P1 to generate GPP1 signal); and

a clock generating circuit that supplies clock signals to said transfer stages in an alternating manner to generate a progressive sequence of scanning pulses (Fig. 7; Col. 11, Ln. 47-48; transfer stages are supplied with clock signal "CKG" and the inverted clock "CKG," to generate a plurality of sequential pulses P1 to P257 and GPP1 to GPP257).

With regarding to **claim 2**, Matsushima discloses the scanning circuit wherein said output circuit logically combines the output signal of a given transfer stage with the input signal to said stage (Fig. 6; AND1-256 circuits; e.g. output signal of transfer stage GS-P or input signal of GS-1 is combined with the output signal GS-1 or input signal of GS-2 to generate GPP1 pulse).

With regarding to **claim 4**, Matsushima discloses the scanning circuit wherein said output circuit performs a logical AND function of the input and output signals of each transfer stage, respectively (Fig. 6; AND1 to AND256).

With regarding to **claim 5**, Matsushima discloses the scanning circuit wherein said transfer stages are divided into two groups, one of which comprises odd-numbered stages of said series and the other of which comprises even-numbered stages of said series (odd-numbered stages are a combination of GS-P and GS-1 and produce odd scanning pulse GPP1; even-numbered stages are a combination of GS-1 and GS-2 and produce even scanning pulse GPP2), and wherein said clock generating circuit supplies clock pulses to said two groups in an alternating manner (Col. 11, Ln. 47-48; transfer stages are supplied with clock signal "CKG" and the inverted clock "CKG," to generate a plurality of sequential pulses P1-P257 and GPP1-GPP257 of Fig. 7).

With regarding to **claim 10**, the claim contains the same limitations as recited in claim 5. Therefore, claim 10 is analyzed and rejected as previously discussed under claim 5.

5. Claim 27 is rejected under 35 U.S.C. 102(e) as being anticipated by Yonemoto et al. (US-6,166,769).

With regarding to **claim 27**, Yonemoto et al. disclose an imaging apparatus, comprising:

an image-sensing device having an array of pixels (Fig. 11; pixels 111; Col. 15, Ln. 55-60).

an output circuit for outputting values from selected pixels in said array (Fig. 11; out put circuit 125; Col. 16, Ln. 65).

a scanning circuit for selecting the pixels in said array (Fig. 11; scanning circuit 124; Col. 22, Ln. 9-11), including a plurality of transfer stages connected in series (Col. 22, Ln. 11-16), each of which receives an input signal and produces a corresponding output signal in response to a clock signal (Input signal phi.HS, Col. 22, Ln. 30-41; in respond to clock HCLK1 and HCLK2, the ½ shift registers 151-1 to 151-6 inherently produce corresponding output signals as shown in Figs. 17 and 18), and an output circuit which logically combines the output signals of said transfer stages with another signal to generate scanning pulses (Fig. 15 shows that the output of ½ shift registers 151-1 to 151-6 are combined to form output phi.S1n-1 to phi.Hn) ; and

a clock generating circuit that supplies clock signals to said transfer stages in an alternating manner to generate a progressive sequence of scanning pulses (Col. 23, Ln. 64-67; Fig. 15 shows that HCLK2 is inverted the first time from inverter 152 and supplied to odd shift register and alternatively inverted the second time from inverter 153 and supplied to even shift register, thereby produce a sequential pulses output as shown in Figs. 17 and 18).

6. Claim 31 is rejected under 35 U.S.C. 102(b) as being anticipated by Hayashi et al. (US-5,818,413).

With regarding **claim 31**, Hayashi et al. disclose a pulse signal generating apparatus comprising:

a transfer stage portion comprising a plurality of transfer stages connected in series (Fig. 1B; Hayashi teaches three different serial connections: the first serial connection comprises first, second, third and fourth shift registers; the second serial connection comprises switch

position b, second shift register, third shift register, and switch position c, and the third serial connection comprises switch position c, third shift register, fourth shift register, and switch position d) said transfer stages each including at least one switch for passing current in a direction in which the transfer stages are connected in series (Fig. 1B; transfer stage/ second, third, fourth shift register each includes switch position b, c, d, respectively. It is inherent that the current must be passed in the direction of each of the second and third serial connection described above because of serial connection-property);

a first pulse generating portion that supplies a first driving pulse to first switch positions in the transfer stage portion at predetermined intervals (Col. 5, Ln. 34-36; the second shift register supplies pulse b of Fig. 2 into switch position b of Fig 1B at a predetermine interval with respect to other a, c, and d pulses as shown in Fig. 2);

a second pulse generating portion that supplies a second driving pulse whose phase is shifted from that of the first driving pulse, at the predetermined intervals (Fig. 2; the third register supplies pulse c which is shifted a predetermine interval from driving pulse c), to second switches of the transfer stages which switches are not included in the first switches (Fig. 1B; switch b is belong to the second shift register and switch c is belong to third shift register); and

an output portion that outputs pulse signals successively from a plurality of gates connected to the transfer stages (Fig. 2; Col. 6, Ln. 21-26; output portion of A2-D2 is identical to A1-D1), at intervals shorter than the predetermined intervals (Fig. 2, predetermined interval a-d, and output interval A1-D1; Col. 6, Ln. 24-26; output intervals of A1-D1 or A2-D2 is shorter than the predetermined interval of pulses a-d).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima.

With regarding to **claim 3**, Matsushima discloses the same subject matter in claim 1 and 2. Except that Matsushima fails to explicitly disclose the scanning circuit wherein each transfer stage comprises a switch that receives the input signal and is activated by one of said clock signals, and a buffer for receiving and holding the input signal when said switch is closed.

Official Notice is taken that it is well known and expected in the art for a transfer stage/ shift register to include a switching transistor responsive to read and write enable signal in order to connect the data I/O to a data-in buffer. Therefore, it would have been obvious to modify the device of Matsushima by having the switch, and a buffer built within the same shift register in order to switch and hold input data in response to the enable read and write signals. Thus, the modifications not only simplify the circuitry but also reduce EM noise.

9. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushima in view of Hayashi (US-5,818,413).

With regarding to **claim 18**, Matsushima teaches a scanning circuit comprising: a plurality of transfer stages connected in series (Fig. 6, GS-P-GS-257) and the output signal having a state related to input signal (Fig. 7, output signals GPP1-GPP256 must relate to input signals P1-P256 because the out put GPP1-GPP256 become high in response to the high leading edges of the input pulses P1-P256). However, Matsushima fails to explicitly disclose that each of the transfer stage includes a switch that receives an input signal in response to a clock signal.

Official Notice is taken that it is well known and expected in the art for a transfer stage/ shift register to include a switching transistor responsive to read/write pulse in order to connect the data I/O to a data-in buffer. Therefore, it would have been obvious to modify the device of Matsushima by having the switch within the same shift register in order to switch and hold input data in response to the enable read and write signals. Thus, the modifications not only simplify the circuitry but also reduce EM noise.

Matsushima further disclose a clock generating circuit that generates a first clock signal (Matsushima; CKG) at a given frequency having a first phase that is applied to the switches in a first group of said transfer stages (Col. 11, Ln. 47-57), to cause said transfer stages to receive an input signal at a time corresponding to said first phase (Matsushima, transfer stages/ shift register GS-P to GS-257 must inherently transceive input data in according to "CKG,/CKG" signal because shift registers are used to hold and transmit data in response to clock signal), and a second clock signal at said given frequency having a second phase different from said first phase (Matsushima; invert CKG) that is applied to the switches in a second group of said transfer stages (Matsushima; invert CKG clock is commonly applied to the second group of transfer stages), to cause said transfer stages in said second group to receive an input signal at a

time corresponding to said second phase (Matsushima, the shift register GS-P to GS-257 must inherently hold and transmit data in according to "CKG,/CKG" signal because of the natural operation of the shift-register); and

an output circuit comprising a sequence of AND gates (Fig. 6, AND1-AND256), each of which receives an output signal from a transfer stage in said first group and a transfer stage in said second group (Fig. 6; output signal of transfer stage GS-P or input signal of GS-1 is combined with the output signal GS-1 or input signal of GS-2 to generate GPP1 pulse), but Matsushima fails to explicitly disclose that each of AND produces a sequence of scanning pulses at a frequency higher than said given frequency. However, the limitations are well known in the art as taught by Hayashi.

In the same field of endeavor, Hayashi teaches a scanning circuit with AND gates output wherein the input clock VCK1 and VCK2 and switch SLT (Figs. 3-5) control the number of pixel lines to be selected in one horizontal period according to the specification of the video signal used (abstract). Hayashi further teaches that by setting 5% duty cycle in VCK1 or VCK2, the frequency of the scanning pulses of output A2-D2 become higher than the clock frequency with the setting of 5% duty cycle as shown in Figs. 3-5 (Col. 6, Ln. 43-46; Col. 7, Ln. 58-61; Col. 8, Ln. 23-6). Moreover, pair of two odd-odd output lines A2 and C2 (Fig. 4), even-even output lines B2 and D2 (Fig. 5) can be selected by setting the switch SLT to open or close (Col. 6, Ln. 56-59; Col. 7, Ln. 50-62; Col. 8, Ln.23-36). In light of the teaching from Hayashi, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the scanning circuit of Matsushima by having one of the input clock set to 5% duty cycle and a switch SLT to open or close as taught by Hayashi in order to provide a higher

frequencies for scanning pulses and additional switching modes to improve the versatility of the scanning circuit.

With regarding to **claim 19**, Matsushima in view of Hayashi discloses the scanning circuit (Col. 11, Ln.24-27, scanning circuit/ driver for LCD) wherein the transfer stages of said first group and the transfer stages of the second group are connected in series in an alternating manner (Matsushima, Fig. 6; serial connection from transfer stages/ registers GS-P to GS-257), such that the output signal of a transfer stage in one group is the input signal of a transfer stage in the other group (Matsushima; Fig. 6 shows that the output signal of GS-P is the inputted into GS-1 and the output signal of GS-1 is also inputted into GS-2).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Mizoguchi et al. (US-6,512,545) disclose a solid state image pickup apparatus for reading pixel signal out at high frame rate.

b) Ishida et al. (US-6,590,611) disclose a solid-state image and methods for vertical scanning circuit sequentially out put signal from vertical read out.

c) Morooka (US-5,200,925) discloses a shift register comprising a switching transistor responsive to write/read enable pulse in order to connect input/output to a data-in buffer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung H. Lam whose telephone number is 571-272-7320. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's primary, NGOC YEN VU can be reached on 571-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HL

04/01/2005

NGOC-YEN VU
PRIMARY EXAMINER